PCF8553

40 × 4 LCD segment driver

Rev. 5 — 28 September 2021 Product data sheet

1 General description

PCF8553 is an ultra low-power LCD segment driver with 4 backplane- and 40 segment-driver outputs, with either an I^2C- or an SPI-bus interface. It comprises an internal oscillator, bias generation, instruction decoding, and display controller.

For a selection of NXP LCD segment drivers, see Table 23.

2 Features and benefits

- Single chip LCD controller and driver with temperature range -40 °C to 85 °C
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, ½, or ⅓
- Internal LCD bias generation with buffers
- 40 segment drives:
  - Up to 20 7-segment numeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 segments/elements
- Auto-incrementing display data and instruction loading
- Versatile blinking modes
- Independent supplies of V_{LCD} and V_{DD}
- Power supply ranges:
  - 1.8 V to 5.5 V for V_{LCD}
  - 1.8 V to 5.5 V for V_{DD}
- Ultra low-power consumption
- 400 kHz I^2C-bus interface
- 5 MHz SPI-bus interface
- Internally generated or externally supplied clock signal

3 Applications

- Metering equipment
- Small appliances
- Consumer healthcare devices
- Battery operated devices
- Measuring equipment

4 Ordering information

Table 1. Ordering Information

Product type Number	Topside mark	Package		
		Name	Description	Version
PCF8553DTT/A	PCF8553D	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4.1 Ordering options

Table 2. Ordering options

Product type Number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PCF8553DTT/AJ	PCF8553DTT/AJ [2]	TSSOP56	reel 13” q1 non dry pack	2000	T_{amb} = -40 °C to +85 °C
	PCF8553DTT/AY	TSSOP56	reel 13” q1 dry pack	2000	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/ packages/

[2] Discontinuation notice 202107021DN - drop-in replacement is PCF8553DTT/AY - this is documented in PCN202102010F01.

5 Block diagram

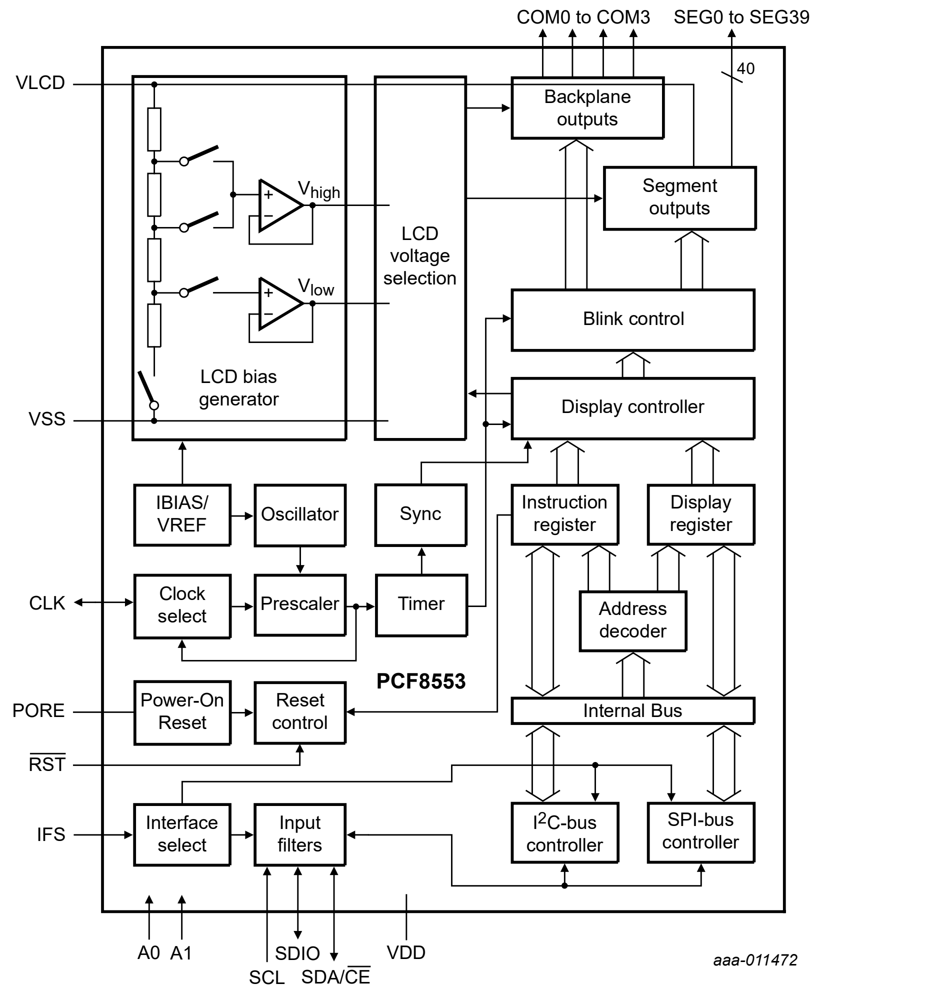


Figure 1. Block diagram of PCF8553

6 Pinning information

6.1 Pinning

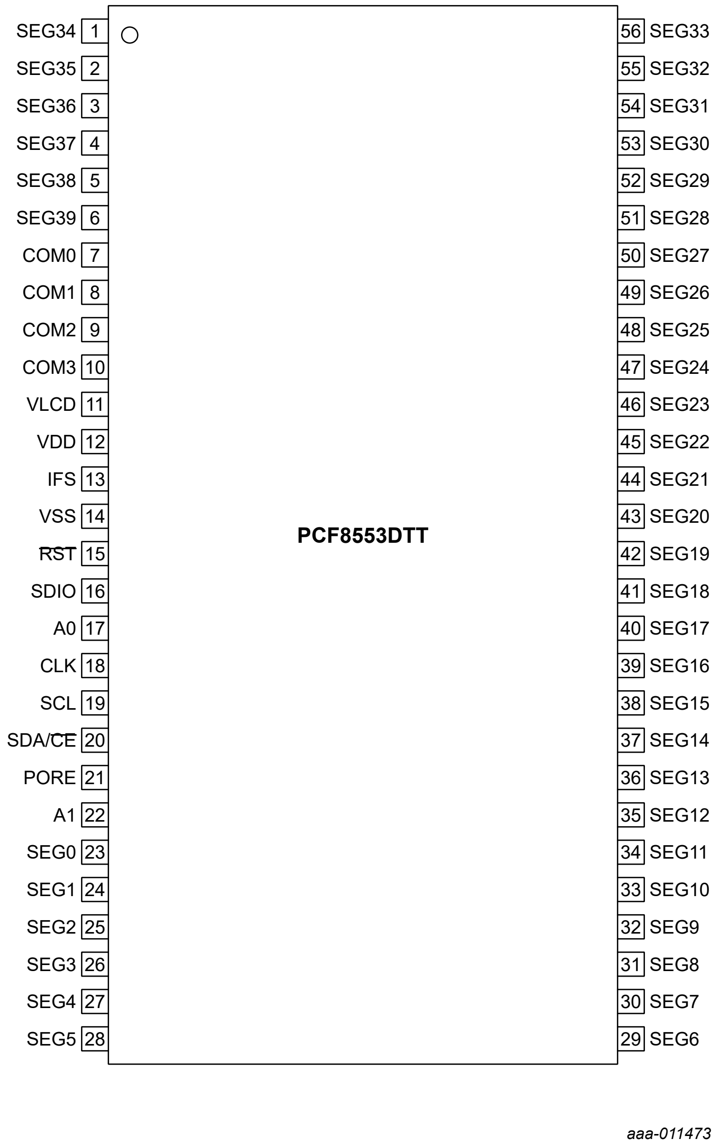


Figure 2. Pin configuration of PCF8553DTT (TSSOP56)

6.2 Pin description

Table 3. Pin description of PCF8553DTT (TSSOP56)

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
Backplane and segment outputs			

Table 3. Pin description of PCF8553DTT (TSSOP56)...*continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
SEG34 to SEG39	1 to 6	output	LCD segments	
SEG0 to SEG33	23 to 56			
COM0 to COM3	7 to 10	output	LCD backplanes	
Supply pins				
VLCD	11	supply	LCD supply voltage	
VDD	12	supply	supply voltage	
VSS	14	supply	ground supply	
Clock and control pins				
$\overline{RST}$	15	input	reset input, active LOW	
PORE[1]	21	input	Power-On Reset (POR) enable • connect to V_{DD} for enabling POR • connect to V_{SS} (or leave open) for disabling POR	
CLK	18	input/output	internal oscillator output, external oscillator input • must be left open if unused	
Bus-related pins			I^2C-bus	**SPI-bus**
IFS[1]	13	input	interface selector input	
			• connect to V_{SS} (or leave open)	• connect to V_{DD}
SDIO	16	input/output	unused	serial data input/output
A0[1]	17	input	hardware device address selection; • connect to V_{SS} (or leave open) for logic 0 • connect to V_{DD} for logic 1	unused
A1[1]	22	input		
SCL	19	input	serial clock input	serial clock input
SDA/$\overline{CE}$	20	input/output	serial data output	chip enable input, active LOW

[1] A series resistance between V_{DD} and the pin must not exceed 1 kΩ to ensure proper functionality, see Section 15.3.

7 Functional description

7.1 Registers of the PCF8553

The registers of the PCF8553 are arranged in bytes with 8 bit, addressed by an address pointer. Table 4 depicts the layout.

Table 4. Registers of the PCF8553

Bits labeled as 0 must always be written with logic 0.

Register name	Address	Bits								Reference
	AP[4:0]	7	6	5	4	3	2	1	0	
Command registers										

Table 4. Registers of the PCF8553*...continued*

Bits labeled as 0 must always be written with logic 0.

Register name	Address	Bits								Reference
	AP[4:0]	7	6	5	4	3	2	1	0	
Software_reset	00h	SR[7:0]								Table 8
Device_ctrl	01h	0	0	0	0	FF[1:0]		OSC	COE	Table 5
Display_ctrl_1	02h	0	0	0	BOOST	MUX[1:0]		B	DE	Table 6
Display_ctrl_2	03h	0	0	0	0	0	BL[1:0]		INV	Table 7
Display data registers[1]										
COM0	04h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	Table 9
	05h	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	06h	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16	
	07h	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24	
	08h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM1	09h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	0Dh	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM2	0Eh	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	12h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	
COM3	13h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	:	:	:	:	:	:	:	:	:	
	17h	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32	

[1] See Table 9.

For writing to the registers, send the address byte first, then write the data to the register (see Section 10.1.4 and Section 10.2.1). The address byte works as an address pointer. For the succeeding registers, the address pointer is automatically incremented by 1 (see Figure 3) and all following data are written into these register addresses. After register 17h, the auto-incrementing will stop and data are ignored.

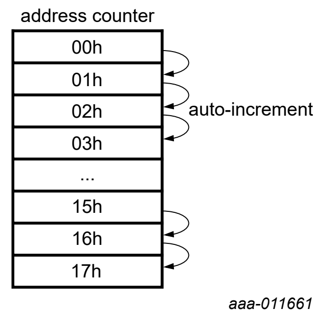


Figure 3. Address counter incrementing

7.2 Command registers of the PCF8553

7.2.1 Command: Device_ctrl

The Device_ctrl command sets the device into a defined state. It should be executed before enabling the display (see bit DE in Table 6).

Table 5. Device_ctrl - device control command register (address 01h) bit description

Bit	Symbol	Value	Description
7 to 4	-	0000	default value
3 to 2	FF[1:0]		**frame frequency selection**
		00	f_{fr} = 32 Hz
		01[1]	f_{fr} = 64 Hz
		10	f_{fr} = 96 Hz
		11	f_{fr} = 128 Hz
1	OSC		**internal oscillator control**
		0[1]	enabled
		1	disabled
0	COE		**clock output enable**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

7.2.1.1 Internal oscillator and clock output

Bit OSC enables or disables the internal oscillator. When the internal oscillator is used, bit COE allows making the clock signal available on pin CLK. If this is not intended, pin CLK should be left open. The design ensures that the duty cycle of the clock output is 50 : 50 (% HIGH-level time : % LOW-level time).

In applications where an external clock has to be applied to the PCF8553, bit OSC must be set logic 1 and COE logic 0. In this case pin CLK becomes an input.

In power-down mode (see Section 7.3.1)

- if pin CLK is configured as an output, there is no signal on CLK
- if pin CLK is configured as an input, the signal on CLK can be removed.

Remark: A clock signal must always be supplied to the device if the display is enabled (see bit DE in Table 6). Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.2.2 Command: Display_ctrl_1

The Display_ctrl_1 command allows configuring the basic display set-up.

Table 6. Display_ctrl_1 - display control command 1 register (address 02h) bit description

Bit	Symbol	Value	Description
7 to 5	-	000	default value
4	BOOST		**large display mode support**
		0[1]	standard power drive scheme
		1	enhanced power drive scheme for higher display loads
3 to 2	MUX[1:0]		**multiplex drive mode selection**
		00[1]	1:4 multiplex drive mode; COM0 to COM3 (n_{MUX} = 4)
		01	1:3 multiplex drive mode; COM0 to COM2 (n_{MUX} = 3)
		10	1:2 multiplex drive mode; COM0 and COM1 (n_{MUX} = 2)
		11	static drive mode; COM0 (n_{MUX} = 1)
1	B[2]		**bias mode selection**
		0[1]	$\frac{1}{3}$ bias (a_{bias} = 2)
		1	$\frac{1}{2}$ bias (a_{bias} = 1)
0	DE		**display enable**[3]
		0[1]	display disabled; device is in power-down mode
		1	display enabled; device is in power-on mode

[1] Default value.
[2] Not applicable for static drive mode.
[3] See Section 7.3.1.

7.2.2.1 Enhanced power drive mode

By setting the BOOST bit to logic 1, the driving capability of the display signals is increased to cope with large displays with a higher effective capacitance. Setting this bit increases the current consumption on V_{LCD}.

7.2.2.2 Multiplex drive mode

MUX[1:0] sets the multiplex driving scheme and the associated backplane drive signals, which are active. For further details, see Section 8.2.

7.2.3 Command: Display_ctrl_2

Table 7. Display_ctrl_2 - display control command 2 register (address 03h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	default value
2 to 1	BL[1:0]		**blink control**
		00[1]	blinking off
		01	blinking on, f_{blink} = 0.5 Hz

Table 7. Display_ctrl_2 - display control command 2 register (address 03h) bit description...*continued*

Bit	Symbol	Value	Description
		10	blinking on, f_{blink} = 1 Hz
		11	blinking on, f_{blink} = 2 Hz
0	INV		**inversion mode selection**
		0[1]	line inversion (driving scheme A)
		1	frame inversion (driving scheme B)

[1] Default value.

7.2.3.1 Blinking

The whole display blinks at frequencies selected by the blink control bits BL[1:0], see Table 7. The blink frequencies are derived from the clock frequency. During the blank-out phase of the blinking period, the display is turned off.

If an external clock with frequency $f_{clk(ext)}$ is used, the blinking frequency is determined by Equation 1. For notation, see Section 8.2.

$$f_{blink(eff)} = \frac{2 \times n_{MUX} \times f_{fr} \times f_{blink}}{f_{clk(ext)}} \quad (1)$$

7.2.3.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The waveforms used to drive LCD inherently produce a DC voltage across the display cell. The PCF8553 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the INV bit.

7.3 Starting and resetting the PCF8553

If the internal Power-On Reset (POR) is enabled by connecting pin PORE to V_{DD}, the chip resets automatically when V_{DD} rises above the minimum supply voltage. No further action is required.

If the internal POR is disabled by connecting pin PORE to V_{SS}, the chip must be reset by driving the $\overline{RST}$ pin to logic 0 for at least 10 µs, see Figure 4. See also application information in Section 15.

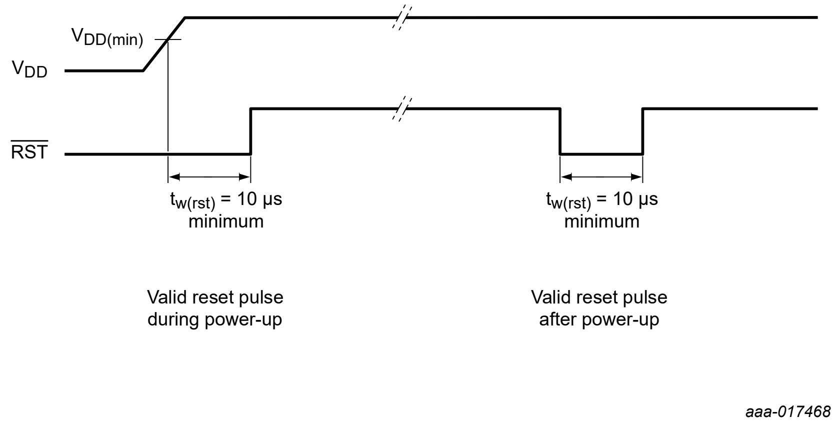


Figure 4. Reset pulse timing

Alternatively a software reset can be applied (see Section 7.3.4).

Following a reset, the register 00h has to be rewritten with 0h by the next command byte or the address pointer AP[4:0] has to be set to the required address after a new START procedure.

7.3.1 Power-down mode

After a reset, the PCF8553 remains in power-down mode. In power-down mode the oscillator is switched off and there is no output on pin CLK. The register settings remain unchanged and the bus remains active. To enable the PCF8553, bit DE (command Display_ctrl_1, see Table 6) must be set to logic 1.

7.3.2 Power-On Reset (POR)

If pin PORE is connected to V_{DD}, the PCF8553 comprises an internal POR, which puts the device into the following starting conditions:

- All backplane and segment outputs are set to V_{SS}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0
- The bus interface is initialized

Remark: The internal POR can be disabled by connecting pin PORE to V_{SS}. In this case, the internal registers are not defined and require a hardware reset according to Section 7.3.3 or a software reset, see Section 7.3.4.

7.3.3 Hardware reset: RST pin

At power-on the PCF8553 can be reset to the following starting conditions by pulling pin $\overline{\text{RST}}$ low:

- All backplane and segment outputs are set to V_{SS}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off

- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0

Remark: The hardware reset overrides the POR see Section 7.3.2.

7.3.4 Command: Software_reset

The internal registers including the display registers and the address pointer (set to logic 0) of the device are reset by the Software_reset command.

Table 8. Software_reset - software reset command register (address 00h) bit description

Bit	Symbol	Value	Description
7 to 0	SR[7:0]		**software reset**
		0000 0000[1]	no reset
		0010 1100	software reset

[1] Default value.

7.4 Display data register mapping

The example in Table 9 and Figure 5 illustrates the segment and backplane mapping of the display in relation to the display RAM.

For example, in 1:4 multiplex drive mode, the backplanes are served by signals COM0 to COM3 and the segments are driven by signals SEG0 to SEG39. Contents of addresses 04h to 08h are allocated to the first row (COM0) starting with the LSB driving the leftmost element and moving forward to the right with increasing bit position. If a bit is logic 0, the element is off, if it is logic 1 the element is turned on. All register content is LSB to MSB left to right. Addresses 09h to 0Dh serve COM1 signals, addresses 0Eh to 12h serve COM2 signals, and addresses 13h to 17h serve COM3 signals.

For displays with fewer segments/elements the unused bits are ignored.

Table 9. Register to segment and backplane mapping

Backplanes[1]	Segments									
	SEG0 to SEG7		SEG8 to SEG15		SEG16 to SEG23		SEG24 to SEG31		SEG32 to SEG39	
	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB
1:4 multiplex drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
COM2	content of 0Eh		content of 0Fh		content of 10h		content of 11h		content of 12h	
COM3	content of 13h		content of 14h		content of 15h		content of 16h		content of 17h	
1:3 multiplex drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
COM2	content of 0Eh		content of 0Fh		content of 10h		content of 11h		content of 12h	
1:2 multiplex drive mode										

Table 9. Register to segment and backplane mapping *...continued*

Backplanes[1]	Segments									
	SEG0 to SEG7		SEG8 to SEG15		SEG16 to SEG23		SEG24 to SEG31		SEG32 to SEG39	
	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	
COM1	content of 09h		content of 0Ah		content of 0Bh		content of 0Ch		content of 0Dh	
static drive mode										
COM0	content of 04h		content of 05h		content of 06h		content of 07h		content of 08h	

[1] See also Section 8.3.1.

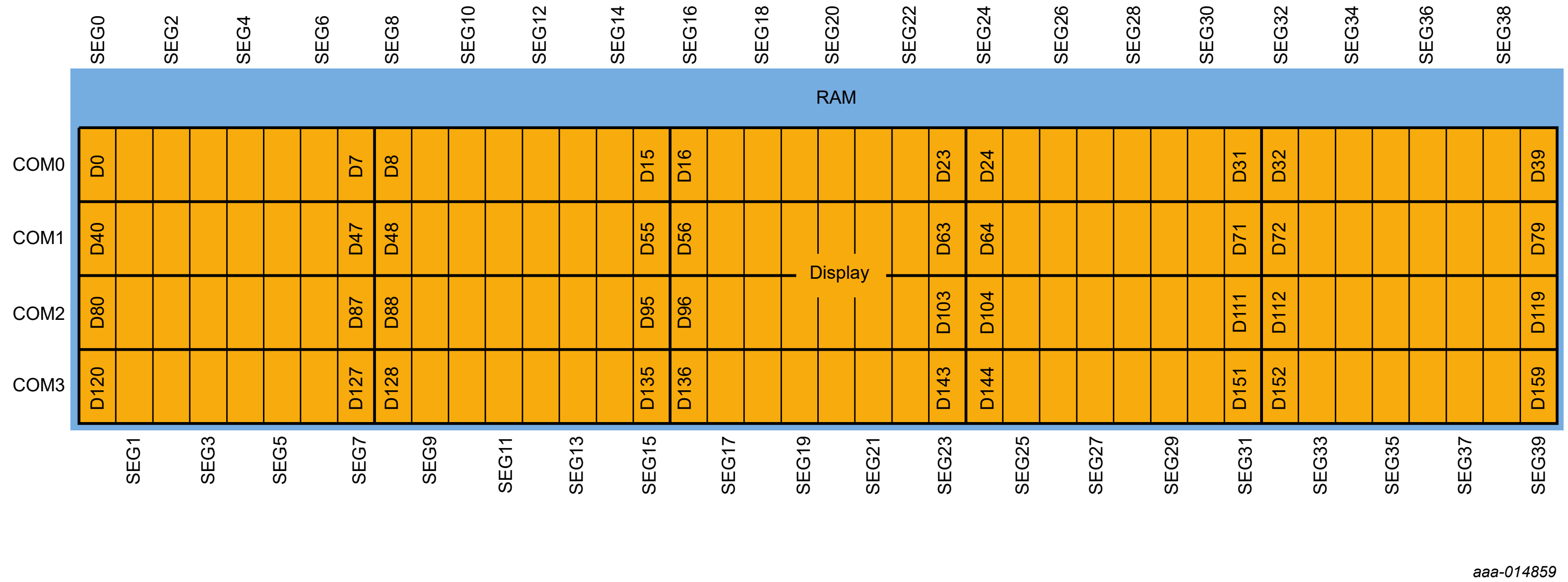


Figure 5. Display RAM organization bitmap for MUX 1:4

8 Possible display configurations

The possible display configurations of the PCF8553 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 10. All of these configurations can be implemented in the typical systems shown in Figure 7 or Figure 8.

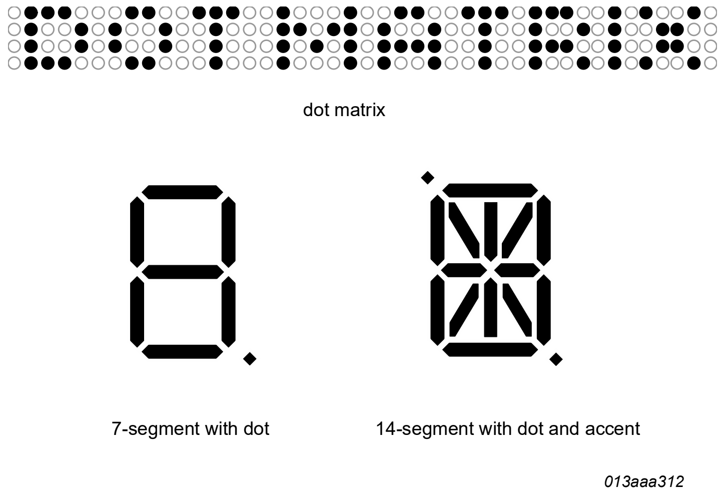
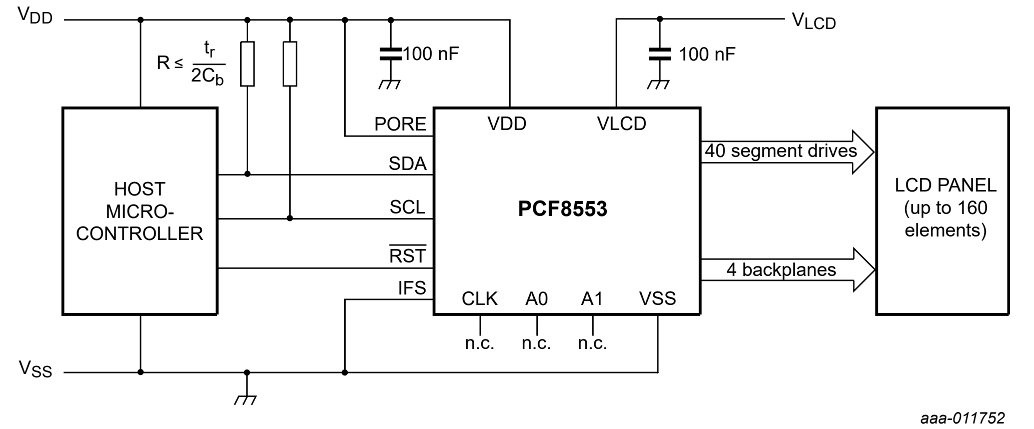


Figure 6. Example of displays suitable for PCF8553

Table 10. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix: segments/ elements**
		7-segment[1]	**14-segment[2]**	
4	160	20	10	160 dots (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 dots (2 × 40)
1	40	5	2	40 dots (1 × 40)

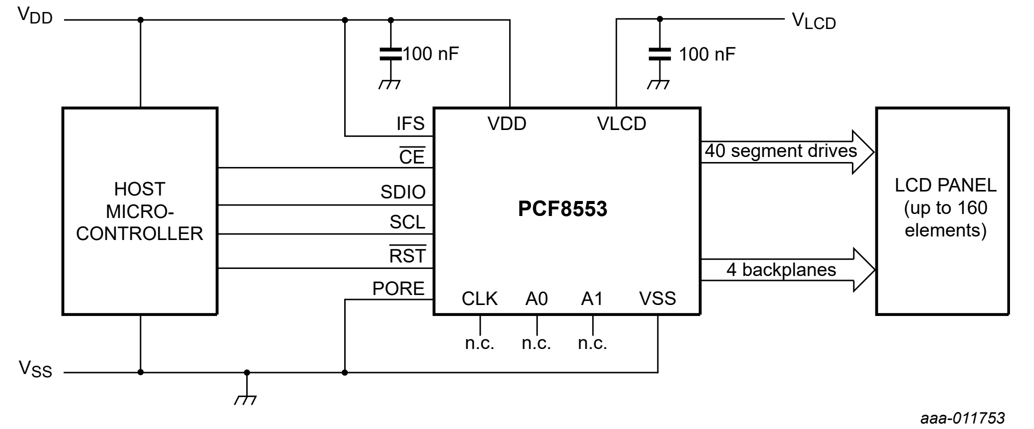
[1] 7 segment display has 8 segments/elements including the decimal point.
[2] 14 segment display has 16 segments/elements including decimal point and accent dot.



The resistance of the power lines must be kept to a minimum. A decoupling capacitor of at least 100 nF is recommended for the supplies.

Figure 7. Typical system configuration using I²C-bus, internal power-on reset enabled

The host microcontroller manages the 2-line I²C-bus communication channel with the PCF8553. The internal oscillator is used and the internal POR is enabled in the example. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the reset, the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.



The resistance of the power lines must be kept to a minimum. A decoupling capacitor of at least 100 nF is recommended for the supplies.

Figure 8. Typical system configuration using SPI-bus, internal power-on reset disabled

The host microcontroller manages the 3-line SPI-bus communication channel with the PCF8553. The internal oscillator is enabled. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are reset, the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

8.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between V_{LCD} and V_{SS}. These intermediate levels are tapped off at positions of ⅓ and ⅔, or ½, depending on the bias mode chosen. To keep current consumption to a minimum, on-chip low-power buffers provide these levels to the display.

8.2 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Display_ctrl_1 command (see Table 6). The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 11.

Table 11. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated with Equation 2

$$\frac{1}{1+a_{bias}} \quad (2)$$

The values for a_{bias} are:

a_{bias} = 1 for ½ bias
a_{bias} = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3:

$$V_{on(RMS)} = \frac{V_{LCD}}{\sqrt{\frac{a_{bias}^2+2a_{bias}+n_{MUX}}{n_{MUX}\times(1+a_{bias})^2}}} \quad (3)$$

where the values for n are

n_{MUX} = 1 for static drive mode
n_{MUX} = 2 for 1:2 multiplex drive mode
n_{MUX} = 3 for 1:3 multiplex drive mode
n_{MUX} = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = \frac{V_{LCD}}{\sqrt{\frac{a_{bias}^2-2a_{bias}+n_{MUX}}{n_{MUX}\times(1+a_{bias})^2}}} \quad (4)$$

Discrimination is a term which is defined as the ratio of the on and off RMS voltages ($V_{on(RMS)}$ to $V_{off(RMS)}$) across a segment. It can be thought of as a measurement of contrast. Discrimination is determined from Equation 5:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a_{bias}^2 + 2a_{bias} + n_{MUX}}{a_{bias}^2 - 2a_{bias} + n_{MUX}}} \quad (5)$$

Using Equation 5, the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

8.2.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 9. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (6)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (7)$$

$V_{on(RMS)}$ (see Equation 3) and $V_{off(RMS)}$ (see Equation 5) are properties of the display driver and are affected by the selection of a_{bias}, n_{MUX}, and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

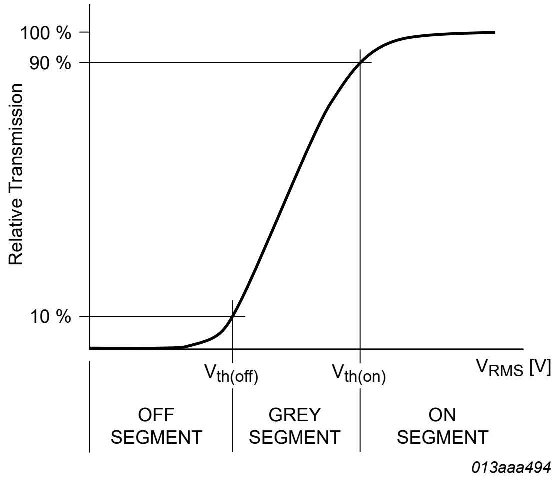
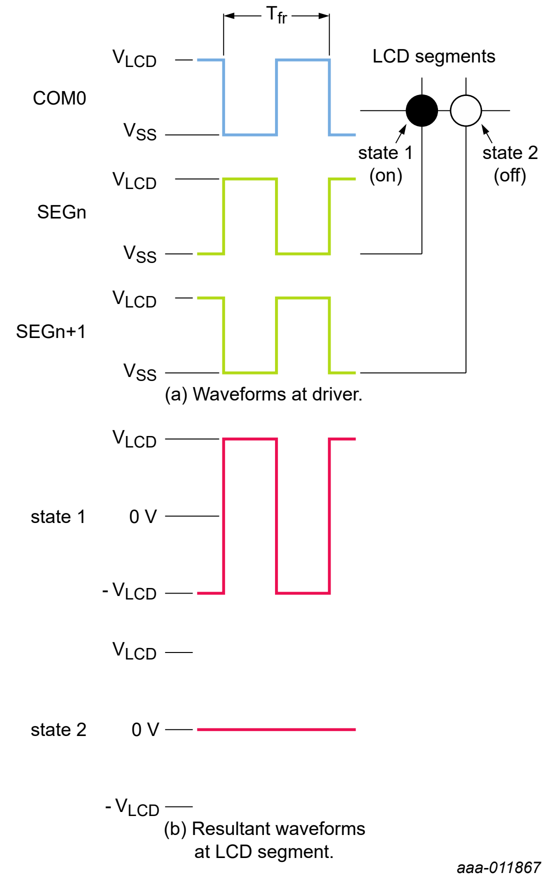


Figure 9. Electro-optical characteristic: relative transmission curve of the liquid

8.2.2 LCD drive mode waveforms

8.2.2.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (COMn) and segment (SEGn) drive waveforms for this mode are shown in Figure 10.

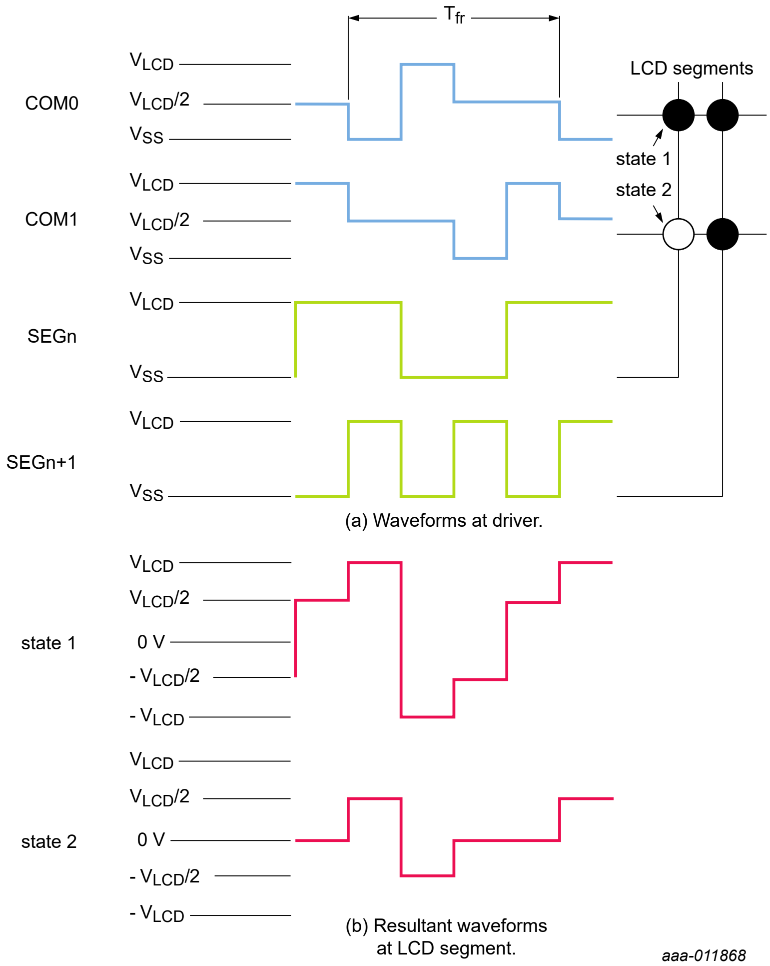


$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.
$V_{on(RMS)} = V_{LCD}$.
$V_{state2}(t) = V_{(SEGn + 1)}(t) - V_{COM0}(t)$.
$V_{off(RMS)} = 0$ V.

Figure 10. Static drive mode waveforms

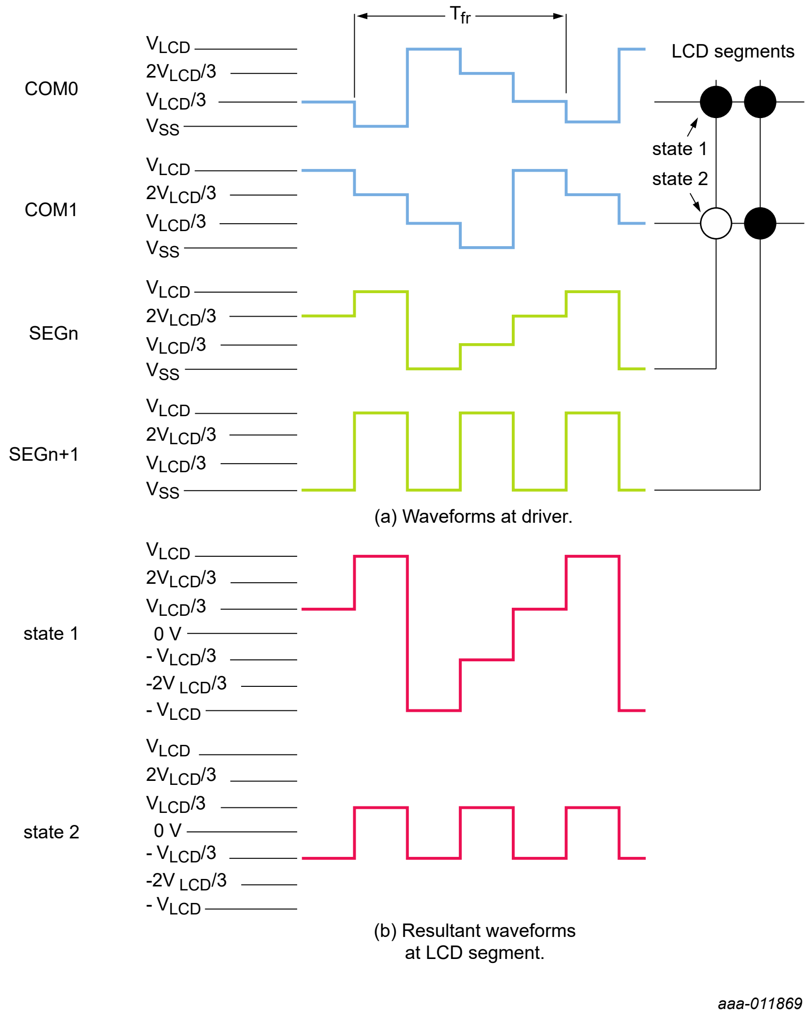
8.2.2.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8553 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in Figure 11 and Figure 12.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.
$V_{on(RMS)} = 0.791V_{LCD}$.
$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.
$V_{off(RMS)} = 0.354V_{LCD}$.

Figure 11. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

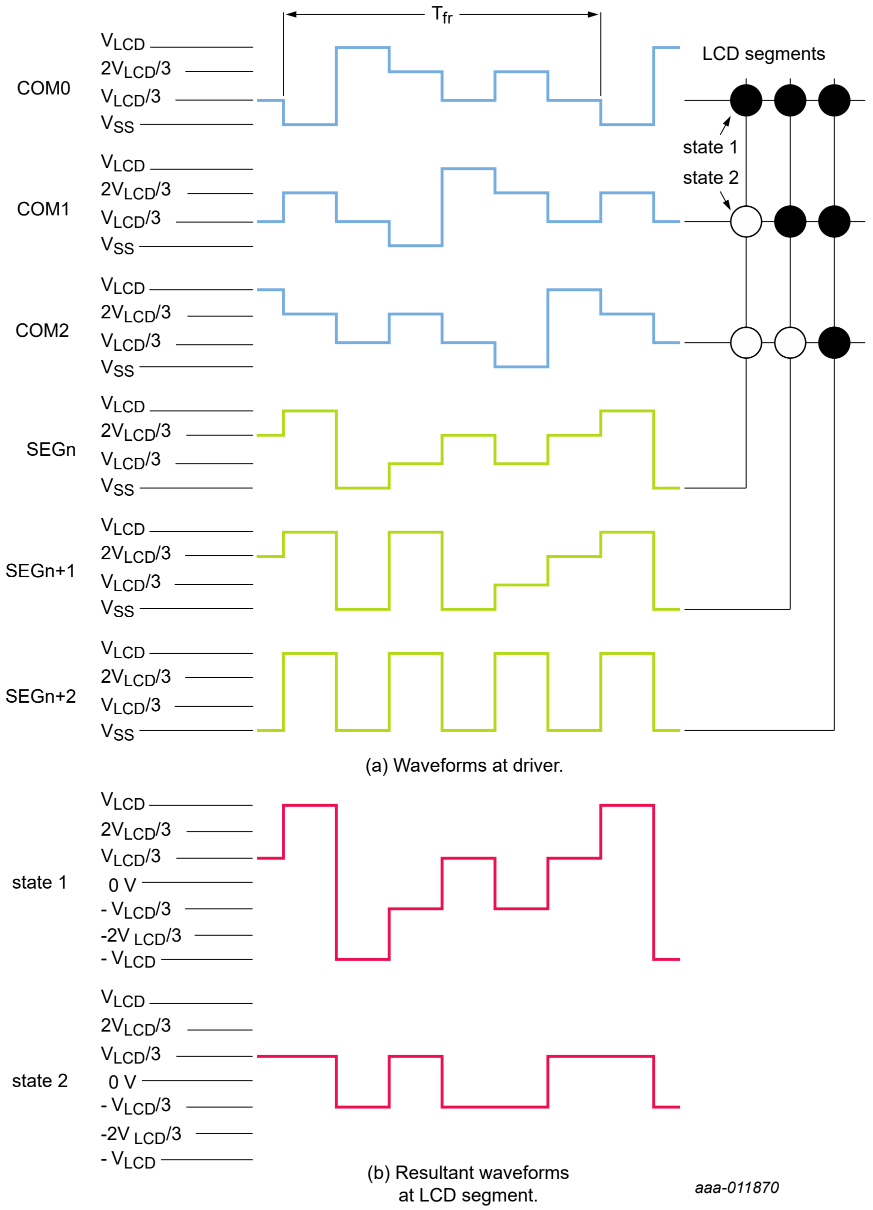
$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Figure 12. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

8.2.2.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 13.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

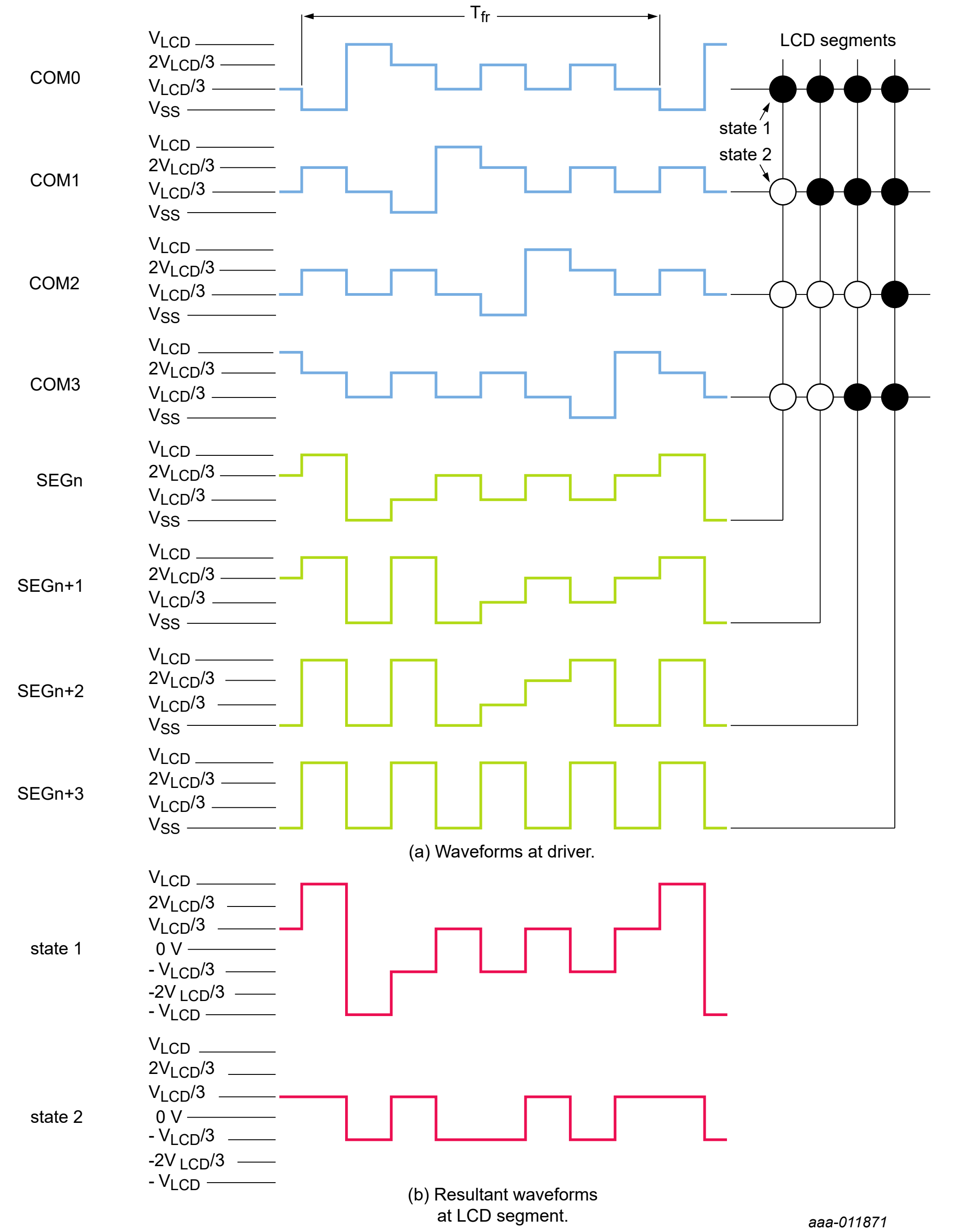
$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Figure 13. Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias

8.2.2.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 14.



$V_{state1}(t) = V_{SEGn}(t) - V_{COM0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{SEGn}(t) - V_{COM1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Figure 14. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias

8.3 Backplane and segment outputs

8.3.1 Backplane outputs

The LCD drive section includes four backplane outputs COM0 to COM3, which must be directly connected to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, COM3 carries the same signal as COM1, therefore these two outputs can be tied together to give enhanced drive capabilities
- In 1:2 multiplex drive mode, COM0 and COM2, respectively, COM1 and COM3 all carry the same signals and may also be paired to increase the drive capabilities
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements

8.3.2 Segment outputs

The LCD drive section includes 40 segment outputs SEG0 to SEG39, which must be directly connected to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display registers. When less than 39 segment outputs are required, the unused segment outputs must be left open-circuit.

9 Power Sequencing

9.1 Power-on

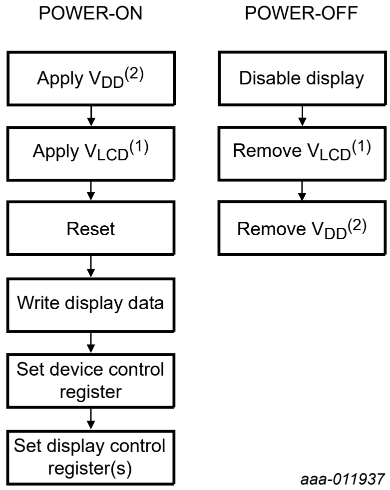
To avoid unwanted artifacts on the display, V_{LCD} must never be asserted before V_{DD}, it is permitted to assert V_{DD} and V_{LCD} at the same time.

9.2 Power-off

Before turning the power to the device off, the display must be disabled by setting bit DE to logic 0. To avoid unwanted artifacts on the display, V_{LCD} must never be connected, while V_{DD} is switched off. It is permitted to switch off V_{DD} and V_{LCD} simultaneously.

9.3 Power sequences

Figure 15 depicts the recommended power-up and power-off sequence.



1. Can be simultaneous with V_{DD}.
2. Can be simultaneous with V_{LCD}.

Figure 15. Recommended power-up and power-off sequence

10 Bus interfaces

10.1 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. Both data and clock lines remain HIGH when the bus is not busy. The PCF8553 acts as a target receiver when being written to and as a target transmitter when being read from.

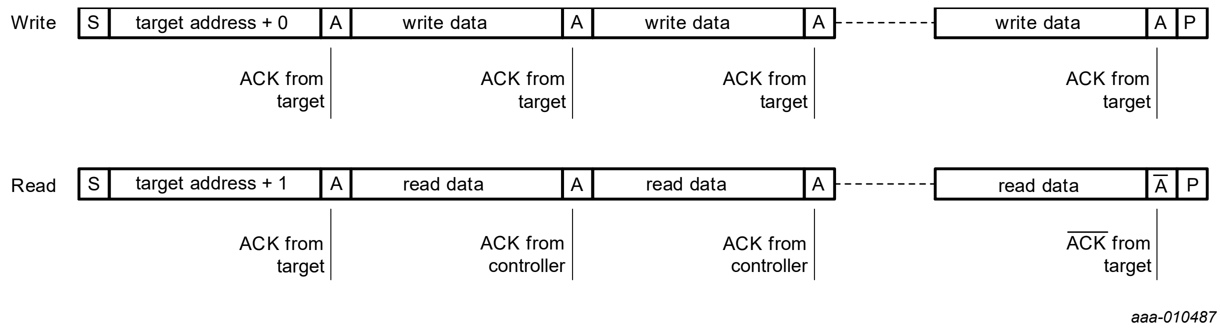


Figure 16. I²C read and write protocol

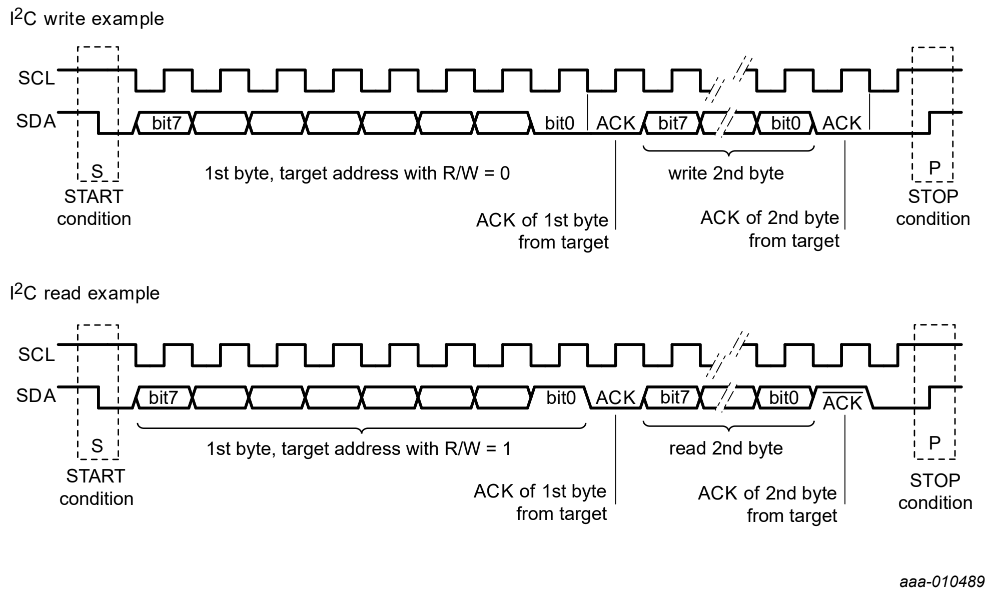


Figure 17. I²C read and write signaling

10.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as STOP or START conditions.

10.1.2 START and STOP conditions

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 17).

10.1.3 Acknowledge

Each byte of 8 bits is followed by an acknowledge cycle. An acknowledge is defined as logic 0. A not-acknowledge is defined as logic 1.

When written to, the target will generate an acknowledge after the reception of each byte. After the acknowledge, another byte may be transmitted. It is also possible to send a STOP or START condition.

When read from, the controller receiver must generate an acknowledge after the reception of each byte. When the controller receiver no longer requires bytes to be transmitted, it must generate a not-acknowledge. After the not-acknowledge, either a STOP or START condition must be sent.

Remark: The PCF8553 omits the not-acknowledge. After the last byte read, the end of transmission is indicated by a STOP or START condition from the controller.

A detailed description of the I²C-bus specification is given in [5].

10.1.4 I^2C interface protocol

The PCF8553 uses the I^2C interface for data transfer. Interpretation of the data is determined by the interface protocol.

10.1.4.1 Write protocol

After the I^2C target address is transmitted, the PCF8553 requires that the register address pointer is defined. It can take the value 00h to 17h. Values outside of that range will result in the transfer being ignored, however the target will still respond with acknowledge pulses.

After the register address has been transmitted, write data is transmitted. The minimum number of data write bytes is 0 and the maximum number is unlimited. After each write, the address pointer increments by one. After address 17h, the address pointer stops incrementing at 18h.

- I^2C START condition
- I^2C target address + write
- start register pointer
- write data
- write data
- :
- write data
- I^2C STOP condition; an I^2C RE-START condition is also possible.

10.1.4.2 Read protocol

When reading the PCF8553, reading starts at the current position of the address pointer. The address pointer for read data should first be defined by a write sequence.

- I^2C START condition
- I^2C target address + write
- start address pointer
- I^2C STOP condition; an I^2C RE-START condition is also possible.

After setting the address pointer, a read can be executed. After the I^2C target address is transmitted, the PCF8553 will immediately output read data. After each read, the address pointer increments by one. After address 17h, the address pointer stops incrementing at 18h.

- I^2C START condition
- I^2C target address + read
- read data (controller sends acknowledge bit)
- read data (controller sends acknowledge bit)
- :

10.1.4.3 I^2C-bus target address

Device selection depends on the I^2C-bus target address. Four different I^2C-bus target addresses can be used to address the PCF8553 (see Table 12).

Table 12. I^2C target address byte

	target address							
Bit	**7 MSB**	**6**	**5**	**4**	**3**	**2**	**1**	**0 LSB**
	0	1	1	1	0	A1	A0	$R/\overline{W}$

The least significant bit of the target address byte is bit $R/\overline{W}$ (see Table 13).

Table 13. R/W-bit description

$R/\overline{W}$	Description
0	write data
1	read data

Bit 1 and bit 2 of the target address are defined by connecting the input pins A0 and A1 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, four instances of PCF8553 can be distinguished on the same I^2C-bus.

10.2 SPI-bus interface

Data transfer to the device is made via a 3-line SPI-bus (see Table 14). There is no dedicated output data line. The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is pulled down.

Table 14. Serial interface

Symbol	Function	Description
$\overline{CE}$	chip enable input[1]; active LOW	when HIGH, the interface is reset
SCL	serial clock input	input may be higher than V_{DD}
SDIO	serial data input/output	input data are sampled on the rising edge of SCL, output data are valid after the falling edge of SCL

[1] The chip enable must not be wired permanently LOW.

10.2.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal $\overline{CE}$. The first byte transmitted is the register address comprising of the address pointer and the $R/\overline{W}$ bit.

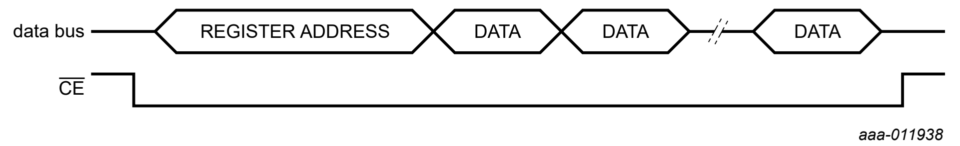


Figure 18. Data transfer overview

Table 15. Address byte definition

Bit	Symbol	Value	Description
7	R/$\overline{\text{W}}$		**data read or write selection**
		0	write data
		1	read data
6 to 5	-	00	default value
4 to 0	AP[4:0]		**pointer to register start address**
		00h to 17h	valid range; other addresses are ignored

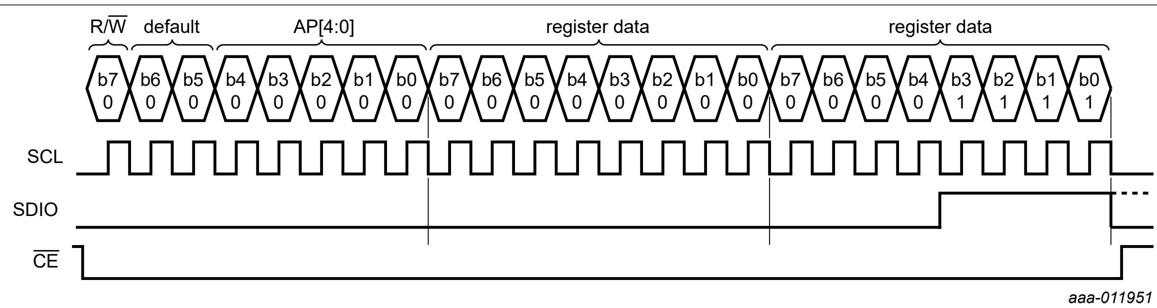
After the register address byte, the register contents follows with the address pointer being auto-incremented after every eighth bit sent (see Section 7.1).

10.2.1.1 Write protocol

After the $\overline{\text{CE}}$ is set LOW, the PCF8553 requires that R/$\overline{\text{W}}$ and the register address pointer is defined. It can take the value 00h to 17h. Values outside of that range will result in the transfer being ignored.

After the register address has been transmitted, write data is transmitted. The minimum number of data write bytes is 0 and the maximum number is unlimited. After each write, the address pointer increments by one. After address 17h, the address pointer stops incrementing at 18h.

- $\overline{\text{CE}}$ set LOW
- R/$\overline{\text{W}}$ = 0 and register address
- write data
- write data
- :
- write data
- $\overline{\text{CE}}$ set HIGH



Data transfers are terminated by de-asserting $\overline{\text{CE}}$ (set $\overline{\text{CE}}$ to logic 1).

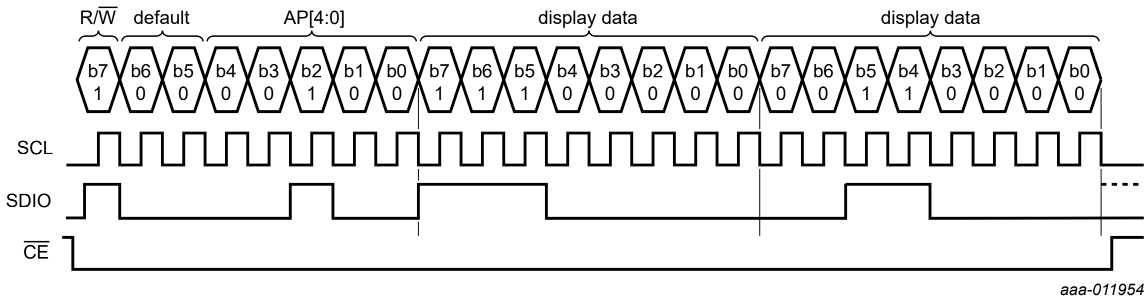
Figure 19. SPI-bus write example: writing two data bytes to registers 00h and 01h

10.2.1.2 Read protocol

When reading the PCF8553, reading starts at the defined position of the address pointer. After setting the address pointer, the read can be executed. After each read, the address pointer increments by one. After address 17h, the address pointer stops incrementing at 18h.

- $\overline{\text{CE}}$ set LOW

- R/$\overline{W}$ = 1 and register address
- read data
- read data
- :
- $\overline{CE}$ set HIGH



Data transfers are terminated by de-asserting $\overline{CE}$ (set $\overline{CE}$ to logic 1).

Figure 20. SPI-bus read example: reading two data bytes from registers 04h and 05h

10.3 EMC detection

The PCF8553 is ruggedized against EMC susceptibility; however it is not possible to cover all cases. To detect if a severe EMC event has occurred, it is possible to check the responsiveness of the device by reading its registers.

11 Internal circuitry

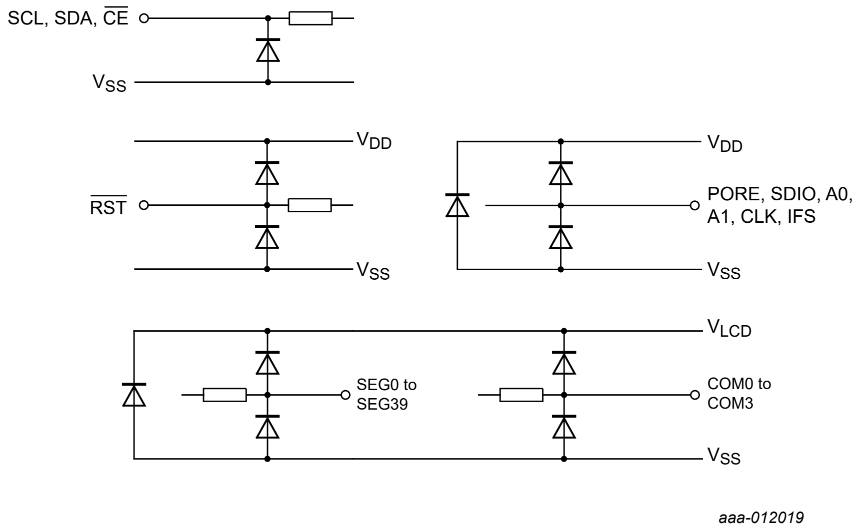


Figure 21. Device protection diagram

12 Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

13 Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.5	V
V_{LCD}	LCD supply voltage			-0.5	+6.5	V
V_I	input voltage			-0.5	+6.5	V
V_O	output voltage			-0.5	+6.5	V
I_I	input current			-10	+10	mA
I_O	output current			-10	+10	mA
I_{DD}	supply current			-50	+50	mA
$I_{DD(LCD)}$	LCD supply current			-50	+50	mA
I_{SS}	ground supply current			-50	+50	mA
P_{tot}	total power dissipation			-	100	mW
P_o	output power			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]			
		on pins SCL and SDA/$\overline{CE}$		-	±2 000	V
		on all other pins		-	±5 000	V
		CDM	[2]	-	±1 500	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	-55	+150	°C
T_{amb}	ambient temperature	operating device		-40	+85	°C

[1] Pass level; Human Body Model (HBM), according to [1].
[2] Pass level; Charged-Device Model (CDM), according to [2].
[3] Pass level; latch-up testing according to [3] at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see [6]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

14 Characteristics

Table 17. Electrical characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 5.5 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

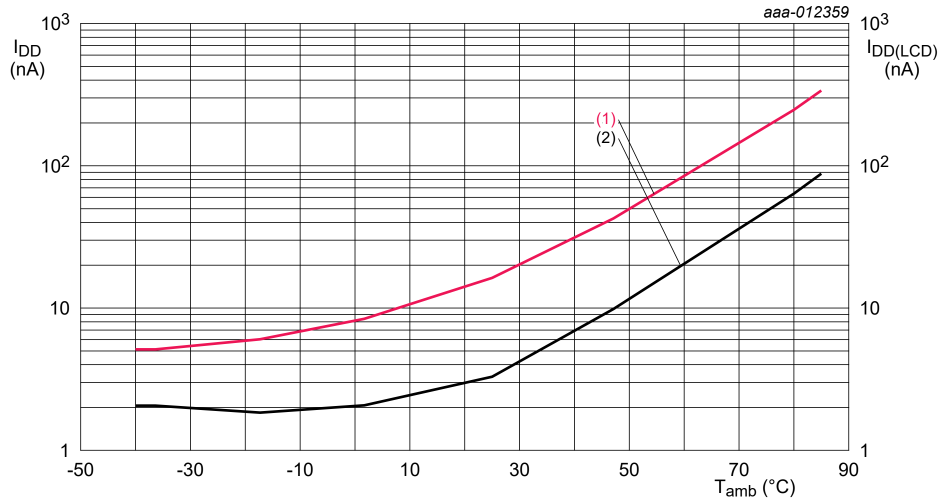
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			1.8	-	5.5	V
I_{DD}	supply current	f_{fr} = 64 Hz; no bus activity					
		V_{DD} = 3.3 V; T_{amb} = 25 °C		-	0.6	-	μA
		V_{DD} = 5.5 V; T_{amb} = 85 °C		-	1.2	2.7	μA
$I_{DD(LCD)}$	LCD supply current	f_{fr} = 64 Hz; no bus activity	[1]				
		V_{LCD} = 5.5 V; T_{amb} = 85 °C; BOOST = 0; no display load		-	3.2	4.5	μA
		V_{LCD} = 3.3 V; T_{amb} = 25 °C					
		BOOST = 0; no display load		-	2.5	-	μA
		BOOST = 0; display enabled; display load C_L = 1.6 nF		-	5.0	-	μA
		BOOST = 1; display enabled; display load C_L = 1.6 nF		-	6.0	-	μA
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		[2]	$0.7V_{DD}$	-	V_{DD}	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V					
		on pin CLK		2	-	-	mA
		on pin SDIO		2	-	-	mA
		on pin SDA		3	-	-	mA
I_{OH}	HIGH-level output current	output source current; on pins SDIO, CLK; V_{OH} = 4.6 V; V_{DD} = 5 V		2	-	-	mA
I_L	leakage current	any input pin except for $\overline{RST}$		-	0	-	nA
		after ESD event		-500	-	+500	nA
$R_{pu(RST\_n)}$	pull-up resistance on pin RST_N			-	100	-	kΩ
LCD outputs (pins SEG0 to SEG39 and COM0 to COM3)							
ΔV_o	output voltage variation	V_{LCD} = 5 V		-100	-	+100	mV

Table 17. Electrical characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 5.5 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_o	output resistance	V_{LCD} = 5 V	[3]	-	1.5	3	kΩ

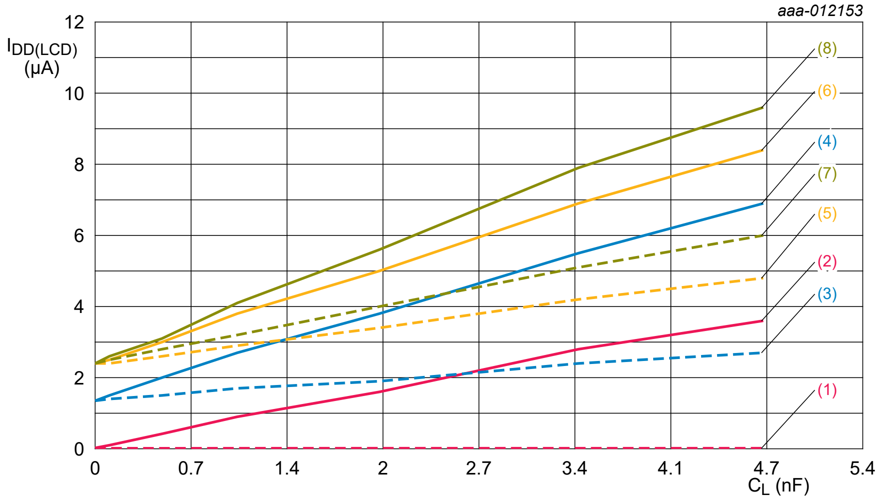
[1] For typical values, also see Figure 22 to Figure 24.
[2] I^2C pins SCL and SDA have no diode to V_{DD} and may be driven up to 5.5 V.
[3] Outputs measured one at a time.



V_{DD} = 5.5 V, V_{LCD} = 5.5 V; power-down mode.

1. I_{DD}.
2. $I_{DD(LCD)}$.

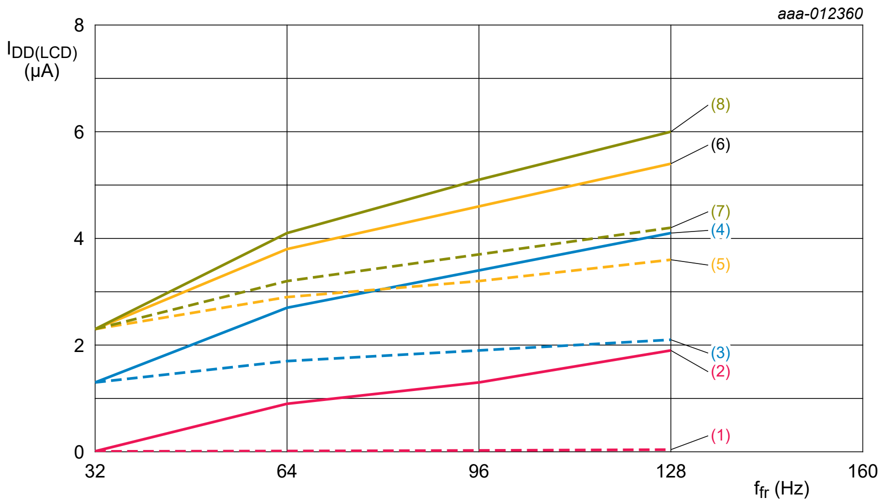
Figure 22. Typical I_{DD} and $I_{DD(LCD)}$ in power-down mode as function of temperature



T_{amb} = 25 °C; V_{LCD} = 3.3 V; V_{DD} = 3.3 V; f_{fr} = 64 Hz, BOOST = 0.

1. Static, all segments/elements off.
2. Static, all segments/elements on.
3. MUX 1:2, bias level $\frac{1}{2}$, all segments/elements off.
4. MUX 1:2, bias level $\frac{1}{2}$, all segments/elements on.
5. MUX 1:3, bias level $\frac{1}{3}$, all segments/elements off.
6. MUX 1:3, bias level $\frac{1}{3}$, all segments/elements on.
7. MUX 1:4, bias level $\frac{1}{3}$, all segments/elements off.
8. MUX 1:4, bias level $\frac{1}{3}$, all segments/elements on.

Figure 23. Typical $I_{DD(LCD)}$ as function of display load



T_{amb} = 25 °C; V_{LCD} = 3.3 V; V_{DD} = 3.3 V; f_{fr} = 64 Hz, BOOST = 0, C_L = 1.6 nF.

1. Static, all segments/elements off.
2. Static, all segments/elements on.
3. MUX 1:2, bias level $^1\!/_2$, all segments/elements off.
4. MUX 1:2, bias level $^1\!/_2$, all segments/elements on.
5. MUX 1:3, bias level $^1\!/_3$, all segments/elements off.
6. MUX 1:3, bias level $^1\!/_3$, all segments/elements on.
7. MUX 1:4, bias level $^1\!/_3$, all segments/elements off.
8. MUX 1:4, bias level $^1\!/_3$, all segments/elements on.

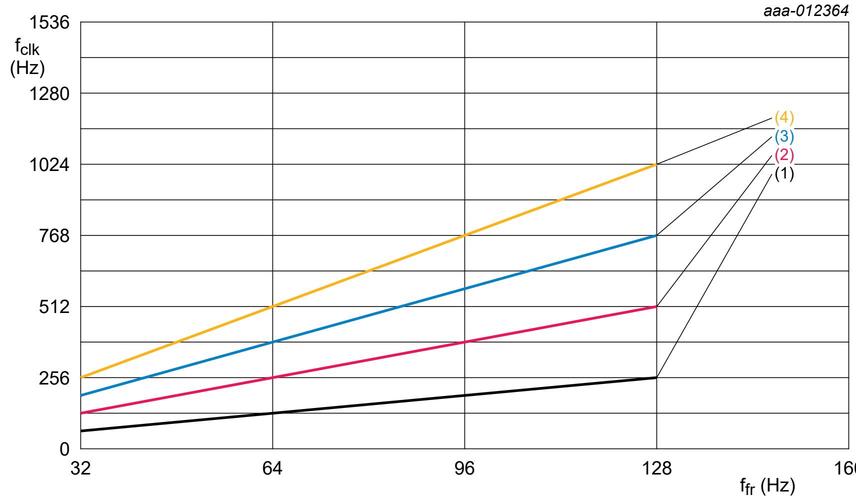
Figure 24. Typical $I_{DD(LCD)}$ as function of f_{fr}

Table 18. Frequency characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 5.5 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{fr}	frame frequency	FF[1:0] = 00		-	32	-	Hz
		FF[1:0] = 01		42	64	86	Hz
		FF[1:0] = 10		-	96	-	Hz
		FF[1:0] = 11		-	128	-	Hz
$f_{clk(int)}$	internal clock frequency	f_{fr} = 64 Hz, n_{MUX} = 4	[1]	-	1024	-	Hz
$f_{clk(ext)}$	external clock frequency		[1]	-	-	4096	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock		60	-	-	μs
$t_{clk(L)}$	LOW-level clock time	external clock		60	-	-	μs
$t_{w(rst)}$	reset pulse width	on pin $\overline{RST}$		10	-	-	μs

[1] $f_{clk(int)} = 2 \cdot f_{fr} \cdot n_{MUX}$ or $f_{clk(ext)} = 2 \cdot f_{fr} \cdot n_{MUX}$ respectively (see Table 5 and Table 6).



1. n_{MUX} = 1.
2. n_{MUX} = 2.
3. n_{MUX} = 3.
4. n_{MUX} = 4.

Figure 25. Relation of frame frequency (f_{fr}), clock frequency (f_{clk}) and multiplex-rate (n_{MUX})

Table 19. I²C-bus characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified; all timing values are valid within the operating supply voltage and T_{amb} range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs

Table 19. I²C-bus characteristics...*continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified; all timing values are valid within the operating supply voltage and T_{amb} range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz		-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on the I²C-bus		-	-	50	ns

[1] The I²C-bus interface of PCF8553 is 5 V tolerant.

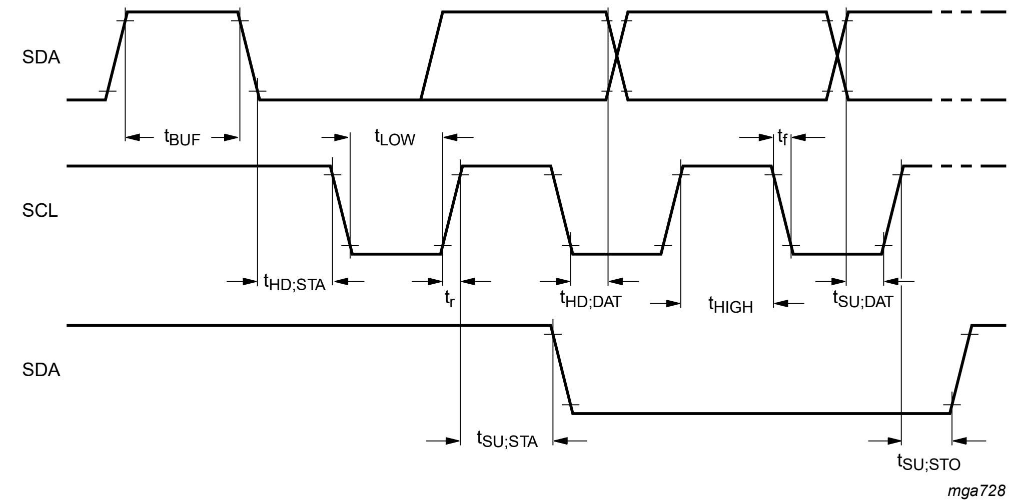


Figure 26. I²C-bus timing waveforms

Table 20. SPI-bus characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified; all timing values are valid within the operating supply voltage and T_{amb} range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	5	MHz
t_{LOW}	LOW period of the SCL clock			150	-	-	ns
t_{HIGH}	HIGH period of the SCL clock			80	-	-	ns
t_r	rise time			-	-	100	ns
t_f	fall time			-	-	100	ns
Pin $\overline{CE}$							

Table 20. SPI-bus characteristics*...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified; all timing values are valid within the operating supply voltage and T_{amb} range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(CE\_N)}$	CE_N set-up time			30	-	-	ns
$t_{h(CE\_N)}$	CE_N hold time			10	-	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time			70	-	-	ns
Pin SDIO							
t_{su}	set-up time	write data		5	-	-	ns
t_h	hold time	write data		50	-	-	ns
$t_{d(R)SDIO}$	SDIO read delay time	C_L = 50 pF		-	-	150	ns
$t_{dis(SDIO)}$	SDIO disable time	no load		-	-	50	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	write to read mode		0	-	-	ns

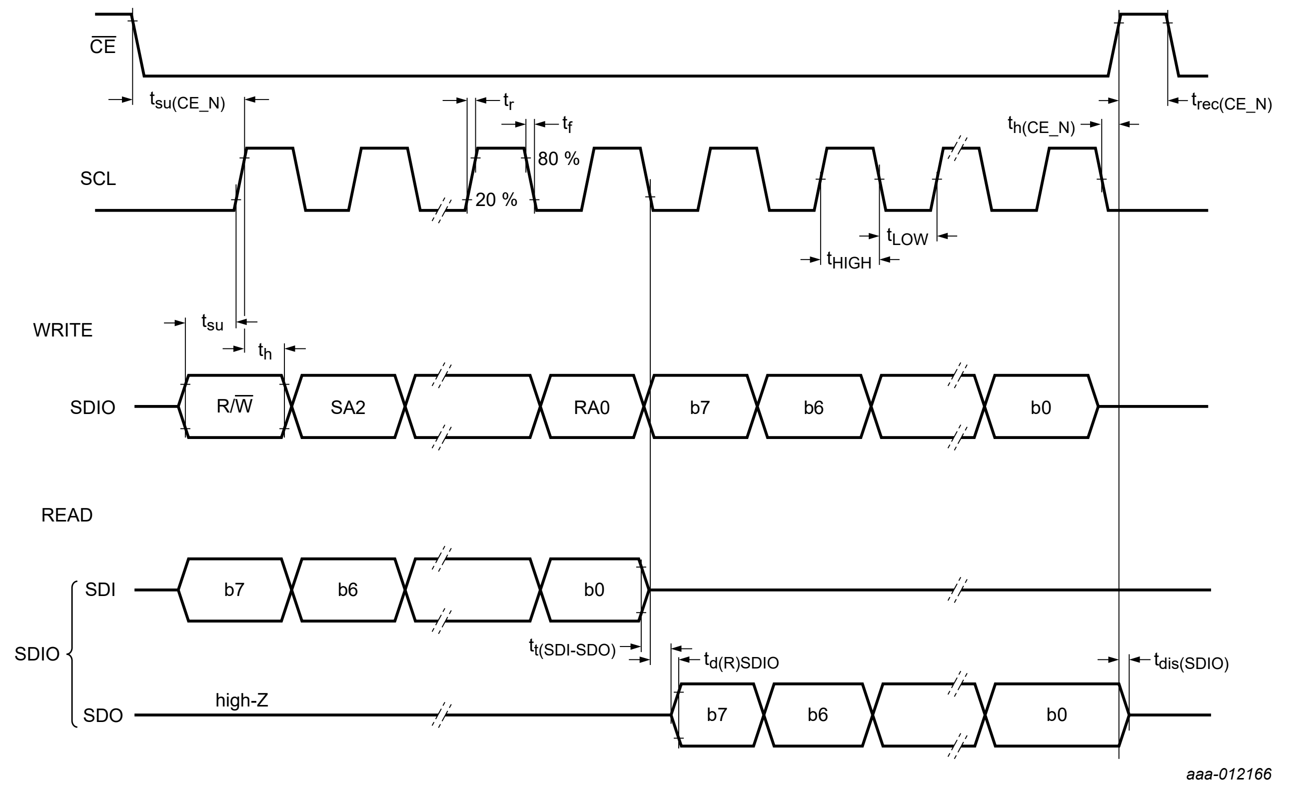


Figure 27. SPI-bus timing waveforms

15 Application information

15.1 Power-on reset

The built-in POR block acts on the rising edge of the V_{DD} supply voltage. Depending on the V_{DD} rising edge in the application, the POR may not work properly. Therefore to ensure proper device operation it is required to send nine clock pulses immediately after power-on (see also UM10204).

15.2 I²C acknowledge after power-on

If the bus does not show an acknowledge at the first access, the command should be sent a second time.

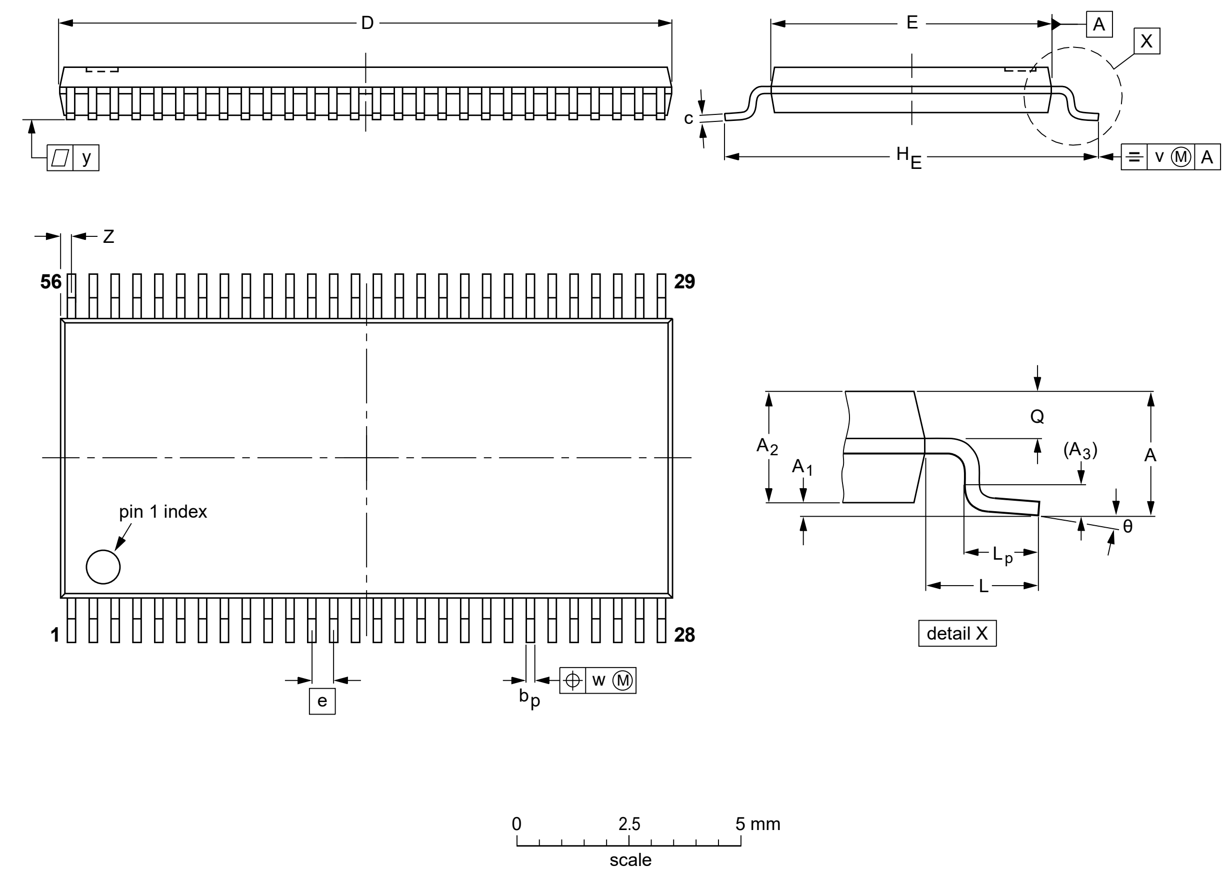
15.3 Resistors on I/O pins

The pins A0, A1, PORE, and IFS comprise internal, latching pull-down devices, which keep these inputs at a low potential when left open. If an input is supposed to be at logic 0 potential, this pin can be either connected to V_{SS} or left open.

In case a pin is supposed to be at logic 1 potential, it must be connected to V_{DD} to avoid any cross-current during power-up. A series resistance between V_{DD} and the associated pin must not exceed 1 kΩ to ensure proper functionality.

16 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Figure 28. Package outline SOT364-1 (TSSOP56) of PCF8553DTT

17 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18 Packing information

18.1 Tape and reel information

For tape and reel packing information, see [4].

19 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages

- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 21 and Table 22

Table 21. SnPb eutectic process (from J-STD-020D)

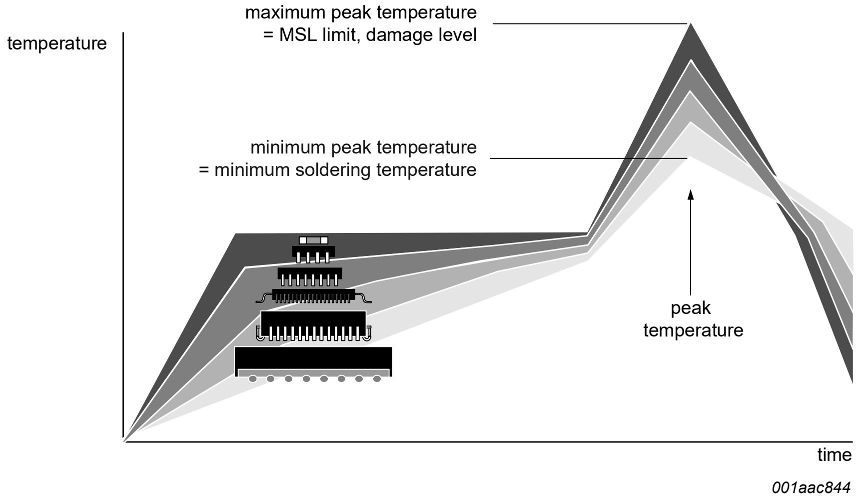
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 22. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.



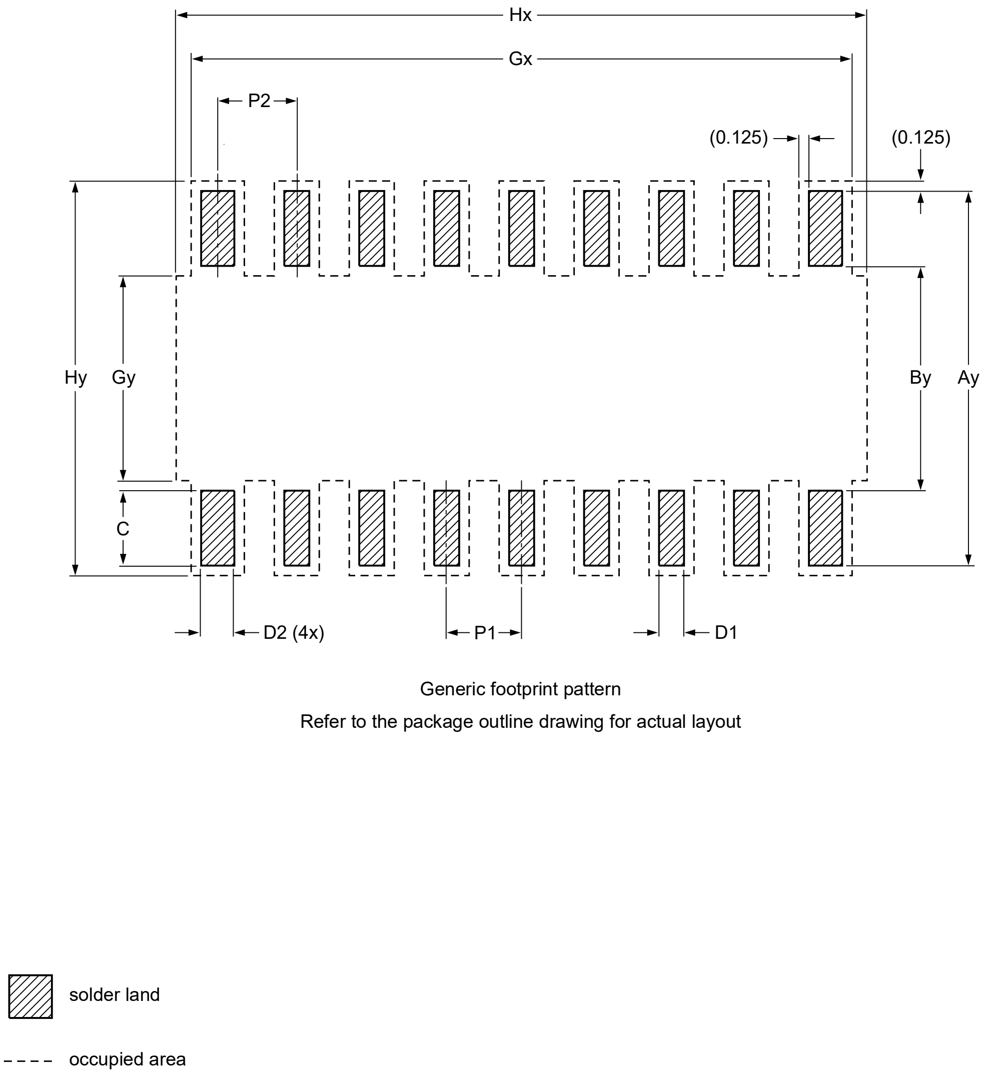
MSL: Moisture Sensitivity Level

Figure 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

20 Footprint information

Footprint information for reflow soldering of TSSOP56 package **SOT364-1**



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	8.900	6.100	1.400	0.280	0.400	14.270	7.000	16.600	9.150

sot364-1_fr

Figure 30. Footprint information for reflow soldering of SOT364-1 (TSSOP56) of PCF8553DTT

21 Appendix

21.1 LCD segment driver selection

Table 23. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	-40 to 105	I²C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 95	I²C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 95	I²C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	-40 to 85	I²C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	-40 to 95	I²C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 105	I²C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	-40 to 85	I²C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	-40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 85	I²C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 95	I²C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	-40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 85	I²C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 95	I²C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 105	I²C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	-40 to 105	I²C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	-40 to 85	I²C	Bare die	N

Table 23. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	-40 to 85	I^2C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	-40 to 105	I^2C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	-40 to 85	I^2C	Bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	-40 to 95	I^2C	Bare die	Y
PCA85233UG	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	-40 to 105	I^2C	Bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	-40 to 85	I^2C	Bare die	N
PCA8530DUG	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	-40 to 105	I^2C / SPI	Bare die	Y
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	-40 to 95	I^2C	Bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	-40 to 95	I^2C	Bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	-40 to 85	I^2C / SPI	Bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	-40 to 105	I^2C / SPI	Bare die	Y

[1] Software programmable.
[2] Hardware selectable.

22 Abbreviations

Table 24. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DC	Direct Current
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface-Mount Device
SPI	Serial Peripheral Interface

23 References

[1] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
[2] JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
[3] JESD78 IC Latch-Up Test
[4] SOT364-1_118 TSSOP56; Reel pack; SMD, 13", packing information
[5] UM10204 I^2C-bus specification and user manual
[6] UM10569 Store and transport requirements

24 Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8553 v.5	20210828	Product data sheet	PCN202102010F01	PCF8553 v.4
Modifications:	• Updated Ordering information. See Change notice column. • Global: The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy.			
PCF8553 v.4	20210420	Product data sheet	202104035I	PCF8553 v.3
Modifications:	• Updated ordering information to new format • Section 7.3 Added "See also application information..." • Section 7.3.2: Added "The bus interface is initialized" • Section 7.3.3: Removed "The bus interface is initialized" • Updated Section 15.1			
PCF8553 v.3	20150327	Product data sheet	-	PCF8553 v.2
Modifications:	• Fixed typo • Added Figure 4			
PCF8553 v.2	20150216	Product data sheet	-	PCF8553 v.1
PCF8553 v.1	20141205	Objective data sheet	-	-

25 Legal information

25.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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